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10/662,725	09/15/2003	Melissa Ann Diercks	138681	1504

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EXAMINER

KRAMSKAYA, MARINA

ART UNIT PAPER NUMBER

2858

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/662,725	<b>Applicant(s)</b> DIERCKS ET AL.	
	<b>Examiner</b> Marina Kramskaya	<b>Art Unit</b> 2858	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 February 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>02/23/2006</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The amended specification and drawings (filed 02/23/2006) omit the signals 161 and 161<sub>N</sub>, which supported the limitation "data is received from at least one of said node *or said breaker*." Currently, the limitation of receiving data from the breaker lacks enablement. Only the limitation of receiving data from the node is enabled for one skilled in the art to make and/or use the invention.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 6-9, 13-14, 18-21, 25, 27, 29, 31, and 33-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Lavoie, US 6,798,209 (prior publication US 2003/0132753).

As per claims 1, 13, 25 and 33, Lavoie discloses a method, an arrangement, and a system of testing an electrical switchgear system, including a storage medium (computer **122**) comprising instructions for controlling a processor for testing, comprising:

applying an analog signal (signal **104** from analog signal generator **103**) to a node (**102**) in said electrical switchgear system (system of FIG. 4), wherein said node monitors a power line signal (**106**, see column 4, lines 32-34) and controls a breaker (**100**) based on said power line signal (**106**), and wherein said analog signal simulates said power line signal (see column 4, lines 63-66); and

receiving data (by computer **122**, through interface **110**) indicative of a response of said electrical switchgear system to said analog signal (see column 5, lines 64-67).

As per Claims 2 and 14, Lavoie discloses a method and an arrangement as applied to claims 1 and 13, above. Lavoie further discloses receiving the data from at least one of said node or said breaker (data is received from breaker **100**).

As per Claims 6 and 18, Lavoie discloses a method and an arrangement as applied to claims 1 and 13, above. Lavoie further discloses applying the analog signal (104) while the node monitors a power line signal (106), (i.e. signal 106 is not isolated from the node 102).

As per Claims 7 and 19, Lavoie discloses a method and an arrangement as applied to claims 1 and 13, above. Lavoie further discloses the analog signals simulating a fault condition of the power line signal (column 5, lines 1-4).

As per Claims 8 and 20, Lavoie discloses a method and an arrangement as applied to claims 1 and 13, above. Lavoie further discloses the analog signals simulating a non-fault condition of the power line signal (column 4, lines 64-65, i.e. a signal which mimics a power line signal broadly includes fault and non-fault conditions).

As per Claims 9 and 21, Lavoie discloses a method and an arrangement as applied to claims 1 and 13, above. Lavoie further discloses modifying the analog signal (column 5, lines 26-28 and 38-40) based on the response, and receiving additional data (by computer 122) representing a further response of said electrical switchgear system (of FIG. 4).

As per Claims 27, 29, 31, and 34, Lavoie discloses a method, an arrangement, storage media, and system as applied to claims 1, 13, 25, and 33 above. Lavoie further

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discloses that the node (102) continues to monitor the power line signal (106) and control the breaker (100) during the application of the analog signal (104) (i.e. signal 106 is not isolated from the node 102).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3-5 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavoie, US 6,798,209 in view of Schweitzer, III, US 5,479,315.

As per Claims 3-5 and 15-17, Lavoie discloses a method and an arrangement as applied to Claims 1 and 13, above.

Lavoie does not explicitly disclose providing an analog signal that

has a magnitude of less than about 10 volts peak-to-peak;

has a magnitude of about 2.5 volts peak-to-peak;

has a magnitude of less than or equal to about 10% of a magnitude of said power line signal.

Schweitzer discloses a method and arrangement for testing a switchgear system wherein an analog signal

has a magnitude of less than about 10 volts peak-to-peak (1.4 Volts);

has a magnitude of about 2.5 volts peak-to-peak (1.4 Volts);

has a magnitude of less than or equal to about 10% of a magnitude of said power line signal (analog signal has a magnitude of 1.4 Volts and power line signal has a magnitude of 70 Volts, hence 2% of the magnitude of the power line signal).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply an analog signal of magnitude that is less than 10 volts, about 2.5 volts, and less than 10% of the power line signal, as taught by Schweitzer, in the method and arrangement of Lavoie, in order to provide a signal that is suitable for electronic processing circuitry.

7. Claims 10-11 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavoie, US 6,798,209 in view of Weeks, US 5,168,261.

As per Claim 10 and 22, Lavoie discloses a method and an arrangement for testing an electrical switchgear system, as applied to claims 1 and 13, above.

Lavoie further discloses having an analog signal (104) as a first analog signal, the node (102) is a first node, the breaker (100) as a first breaker, and the power line signal (106) as a first power line signal.

Lavoie does not explicitly disclose

wherein the method further comprises applying, simultaneously with the application of the first analog signal, a second analog signal to a second node in the electrical switchgear system,

wherein the second node monitors a second power line signal and controls a second breaker based on the second power line signal, and

wherein the second analog signal simulates the second power line signal.

Weeks discloses

applying a second analog signal (from **18**) to a second node (**14** "circuit breaker control #2") in the electrical switchgear system,

wherein the second node (**14** "circuit breaker control #2") monitors a second power line signal (from transmission line **3**) and controls a second breaker (**6** "circuit breaker #2") based on the second power line signal (from transmission line **3**).

Although Lavoie does not explicitly disclose simultaneous application of first and second signal or the second analog signal simulating the second power line signal, it would have been obvious to a person of ordinary skill in the art to replicate the system of Lavoie, wherein a second analog signal would simulate a power line signal, as does the first analog signal (**104**), in order test multiple nodes and multiple breakers in a switchgear system.

Therefore, it would have been obvious to a person of ordinary skill in the art to include multiple nodes and multiple circuit breakers as taught by Weeks, in the system of Lavoie, in order to test multiple nodes and multiple breakers in a switchgear system.



As per Claims 11 & 23, Lavoie discloses a method and an arrangement of testing an electrical switchgear system, as applied to Claims 1 and 13, above.

Lavoie does not explicitly disclose measuring a time required for the said breaker to trip based on timestamps of said data.

Weeks discloses the method and arrangement for testing an electrical switchgear system, further comprising measuring a time required for the said breaker to trip based on timestamps of said data (column 5, lines 16-21).

Therefore, it would have been obvious to a person of ordinary skill in the art to measure a trip time, as taught by Weeks, in the system of Lavoie, in order set proper delay times for resetting the breaker.

8. Claims 12, 24, 26, 28, 30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavoie, US 6,798,209 in view of Weeks, US 5,168,261, and Schweitzer, III, US 5,479,315.

As per Claims 12, 24, and 26 Lavoie discloses a method and an arrangement of testing an electrical switchgear system (of FIG. 4), including a storage medium (computer **122**) comprising instructions for controlling a processor for testing, comprising:

applying a first analog signal (signal **104** from analog signal generator **103**) to a first node (**102**) in said electrical switchgear system (system of FIG. 4), wherein said first node monitors a first power line signal (**106**, see column 4, lines 32-34) and controls a

first breaker (100) based on said first power line signal (106), and wherein said first analog signal simulates said first power line signal (see column 4, lines 63-66);

receiving data (by computer 122, through interface 110) from said first node indicative of a response of said electrical switchgear system to said first analog signal (see column 5, lines 64-67).

Lavoie does not explicitly disclose

applying, simultaneously with said applying said first analog signal, a second analog signal to a second node in said electrical switchgear system, wherein said second node monitors a second power line signal and controls a second breaker based on said second power line signal, and wherein said second analog signal simulates said second power line signal; and

wherein said first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said first power line signal.

Weeks discloses a method and arrangement for testing a switchgear system (ABS.) wherein a second analog signal (from 18) is applied to a second node (14 "circuit breaker control #2" through module 24) in an electrical switchgear system, wherein said second node monitors a second power line signal (from transmission line 3) and controls a second breaker (6 "circuit breaker #2") based on said second power line signal.

Hence, it would have been obvious to a person of ordinary skill in the art to include multiple nodes and multiple circuit breakers as taught by Weeks, in the system of Lavoie, in order to test multiple nodes and multiple breakers in a switchgear system.

It would further be obvious to replicate the system of Lavoie, wherein a second analog signal would simulate a power line signal, as does the first analog signal (104), in order to test multiple nodes and multiple breakers in a switchgear system.

Schweitzer discloses a method and arrangement for testing a switchgear system wherein a first analog signal has a magnitude of less than or equal to about 10% of a magnitude of said power line signal (analog signal has a magnitude of 1.4 Volts and power line signal has a magnitude of 70 Volts, hence 2% of the magnitude of the power line signal).

Therefore, it would have been obvious to a person of ordinary skill in the art to apply an analog signal of magnitude that is less than 10% of the power line signal, as taught by Schweitzer, in the method and arrangement of Lavoie, in order to provide a signal that is suitable for electronic processing circuitry.

As per Claims 28, 30, and 32, Lavoie further discloses that the node (102) continues to monitor the power line signal (106) and control the breaker (100) during the application of the analog signal (104) (i.e. signal 106 is not isolated from the node 102).

### ***Response to Arguments***

9. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tiemann et al., US 6,472,882, discloses a test for a switchgear system with a simulated power line signal.

11. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 02/23/2006 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.


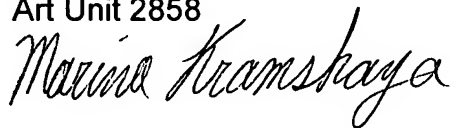
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on (571)272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MK

Marina Kramskaya  
Examiner  
Art Unit 2858



DIANE LEE  
SUPERVISORY PATENT EXAMINER